IN THE SPECIFICATION:

Please substitute the following paragraphs of the specification with the same-numbered paragraphs in the application.

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Paragraph [0020] Figure 2 is a computer system diagram according to the present invention;

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Paragraph [0025] Referring now to the drawings, and more particularly to Figures [[1-3]] 1 through 4, there are shown preferred embodiments of the method and system according to the present invention. Specifically, in the flow diagram illustrating a preferred method of the present invention shown in Figure 1, the method for performing parasitic extraction method comprises the steps of calculating 100 the minimum output impedance for a network-connected component comprising a plurality of ports 607 thereby producing a labeled impedance, estimating 200 the minimum output impedance for every net 605 of an integrated circuit device 610 based on the calculating step 100, comparing 300 the labeled impedance with the estimated impedance, and selecting 400 the net which needs to be extracted based on a ratio of values of the labeled impedance and the estimated impedance.

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Paragraph [0030] A representative hardware environment for practicing the present invention is depicted in Figure 3, which illustrates a typical hardware configuration of an information handling/computer system in accordance with the present invention, having at least

one processor or central processing unit (CPU) 10. The CPUs 10 are interconnected via system bus 112 to random access memory (RAM) 14, read-only memory (ROM) 16, an input/output (I/O) adapter 18 for connecting peripheral devices, such as disk units 111 and tape drives 113, to bus 112, user interface adapter 19 for connecting keyboard 15, mouse 17, speaker 103, microphone 104, and/or other user interface devices such as touch screen device (not shown) to bus 112, communication adapter 105 for connecting the information handling system to a data processing network, and display adapter 101 for connecting bus 112 to display device 102. A program storage device readable by the disk or tape units is used to load the instructions, which operate the invention which is loaded onto the computer system 500.

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Paragraph [0034] An example of this process is presented in Figure 4, which illustrates a simple FET logic circuit 50. The devices a, b are PFETs, and the devices c, d, are NFETs. The circuit 50 further comprises ~~of~~ power supply nodes 1, 2, input nodes 3, 4, and output ~~nodes 5, 6~~ node 5. The power supply nodes 1, 2 are connected to the device ports 11, 21, 43. The device impedances on these ports 11, 21, 43 have no resistance, and only have a capacitance. The input nodes 3, 4 are connected to the device (gate) ports 12, 22, 32, 42. These port impedances have infinite resistance and significant capacitances. ~~The output ports 4, 5 are connected to the device ports 13, 23, 31 and 33, 41.~~ The capacitance on ports 33, 41 is the source capacitance of device c and the drain capacitance of the device d, respectively. The resistances are found in the following manner. Port 41 is connected to power supply node 2 (ground) through the NFET d. Port 41 is connected to power supply node 1 through FET a, or alternatively, FETs b, c. If the sum of the a+c device resistance is larger than the resistance of device d alone, then the device d

will be used for the impedance on port 41.